



GaN electronic devices

Elison Matioli

Institute of Electrical and Micro-engineering

Power and Wide-band-gap Electronics Research (POWERlab)

Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland

Lateral radio frequency (RF) devices

Material Properties of Microwave Semiconductors

	Si	InP	GaAs	SiC	InN	GaN	AlN	Diamond
Egap (eV)	1.1	1.34	1.43	3.3 (4H)	0.63	3.4	6.1	5.5
Electron mobility (cm ² /V·s)	1,350	12,000*	8,500*	900	3,300	2,000*	1,100	1,900
2DEG density (×10 ¹³ cm ⁻²)	N/A	0.3*	<0.2	N/A	N/A	>2	N/A	N/A
Electron effective mass	0.26	0.08	0.067	0.29	0.11	0.2	0.4	1.4
Saturation velocity (×10 ⁷ cm/s)	1	3.3	1	2	3.5	1.5–2.5	1.5	1.9
Critical electric field (MV/cm)	0.3	0.5	0.4	3	1	3.3	6–15	10
Thermal conductivity (W/cm·K)	1.3	0.7	0.5	4.9	1.2	2	2	6–20
Relative dielectric constant	12	12.5	13	9.8	15.3	9.5	9	5.7

* Measured on InAlAs/InGaAs, AlGaAs/InGaAs, AlGaN/GaN HEMT structures.

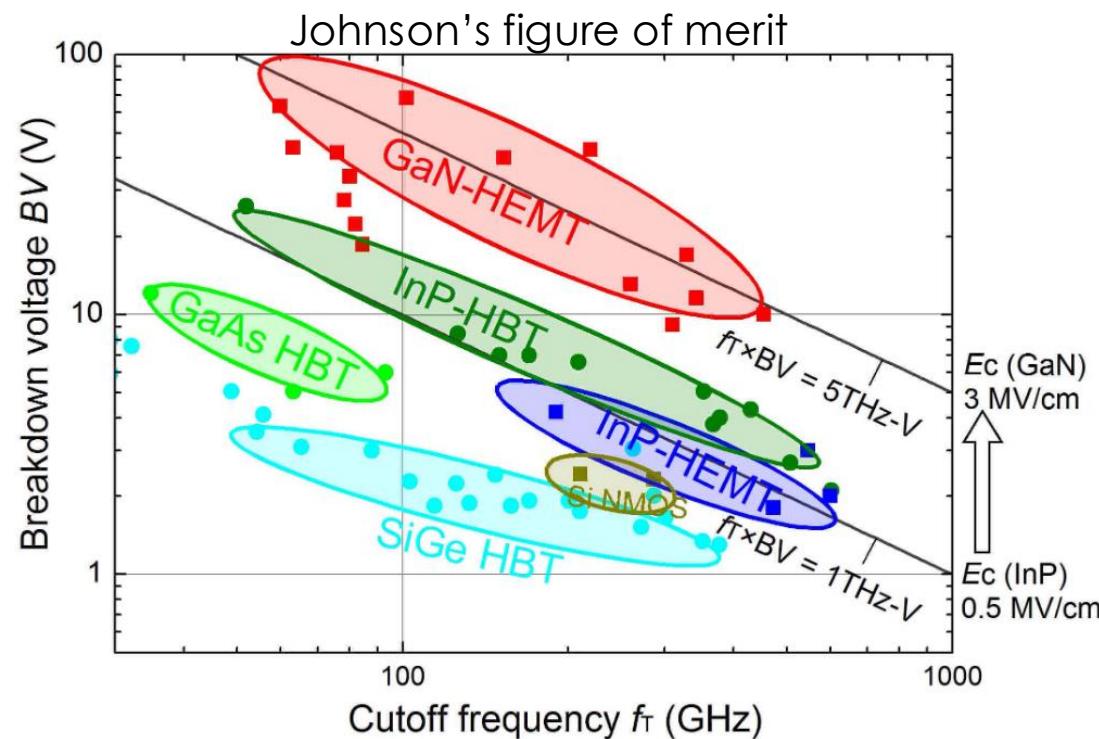
III_Nitrides: Unique combination of high breakdown field, high electron velocity, and large sheet electron densities offers simultaneous high bandwidth and breakdown voltage. Thermal characteristics are enhanced using high thermal conductivity SiC substrates.

GaN HEMTs enable power amplifiers (PAs) with high power added efficiency, significantly higher output power and power density than in GaAs or InP.

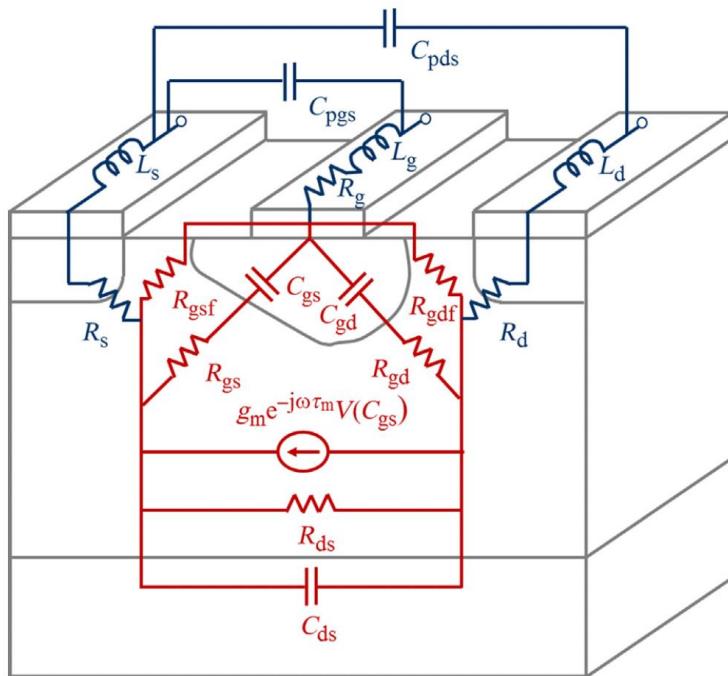
For RF and mixed-signal applications:

f_T , f_{max} , maximum drain current and breakdown voltage (BV) are key device performance parameters.

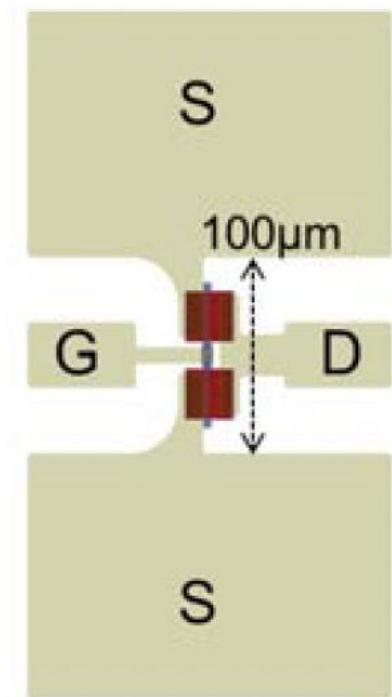
Device scaling successfully increases f_T and f_{max} of GaN transistors but simultaneously deteriorated BV due to small dimension. Low BV greatly restricts the dynamic range of the circuit and represents a severe limitation.



Principles of high frequency devices

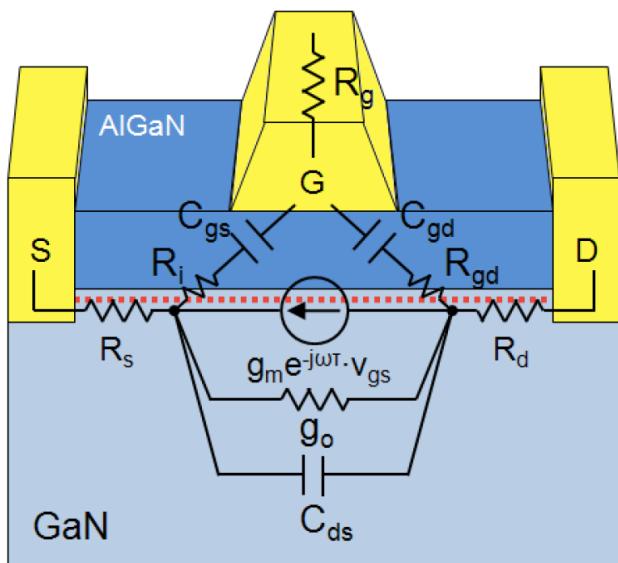


RF contacts

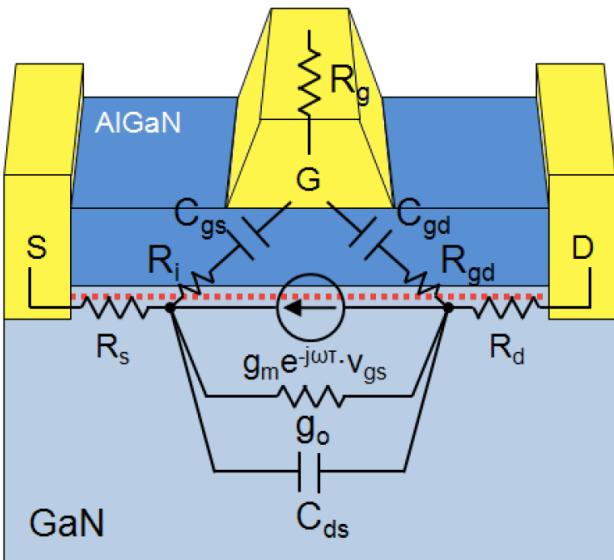
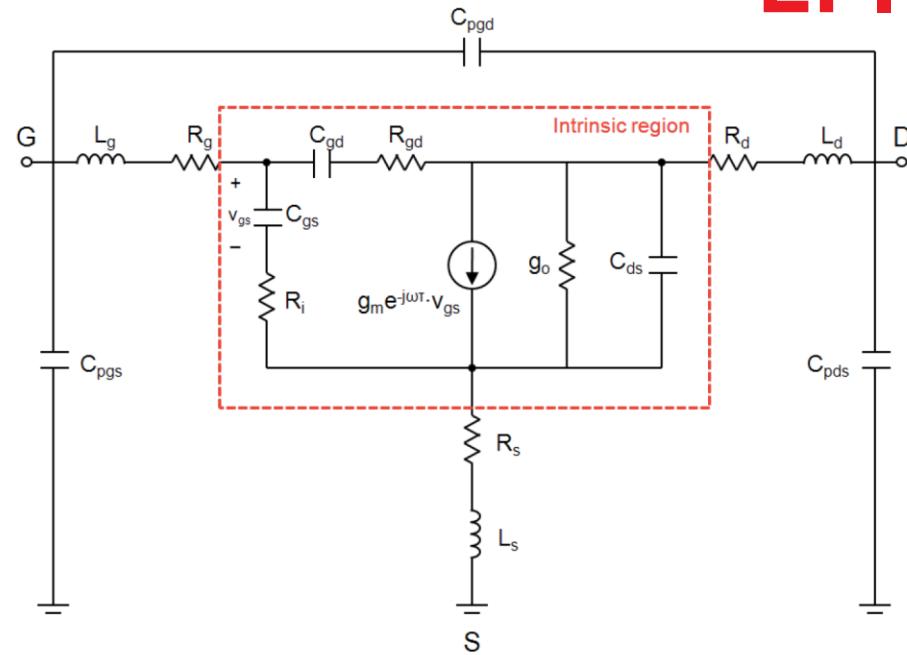
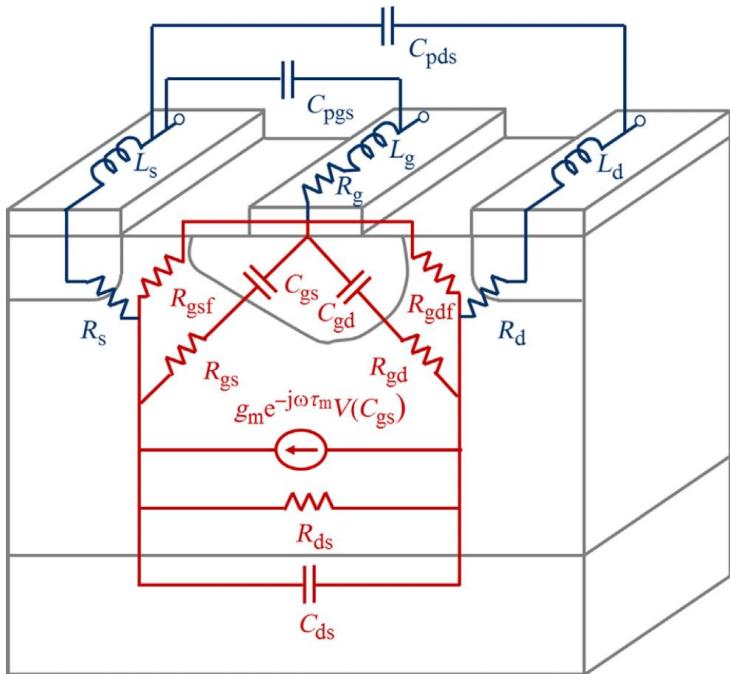


Port 1

Port 2



Principles of high frequency devices

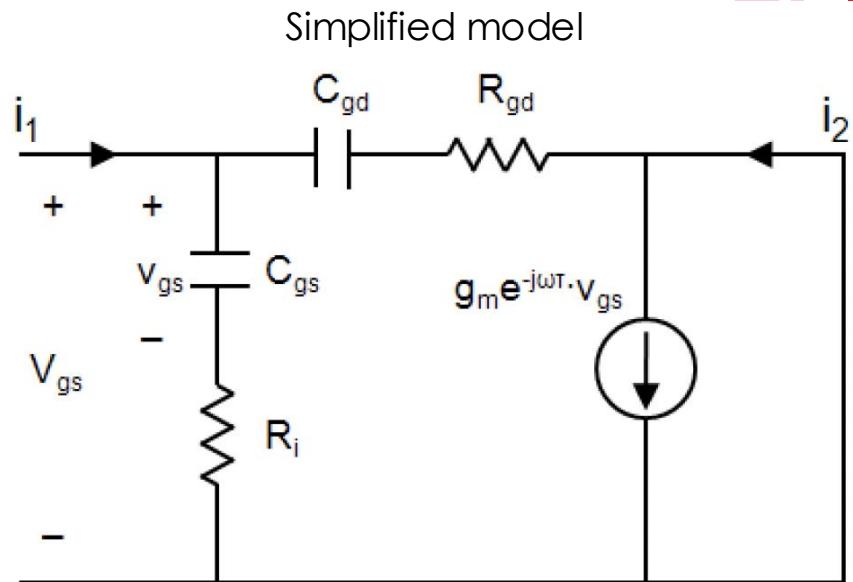
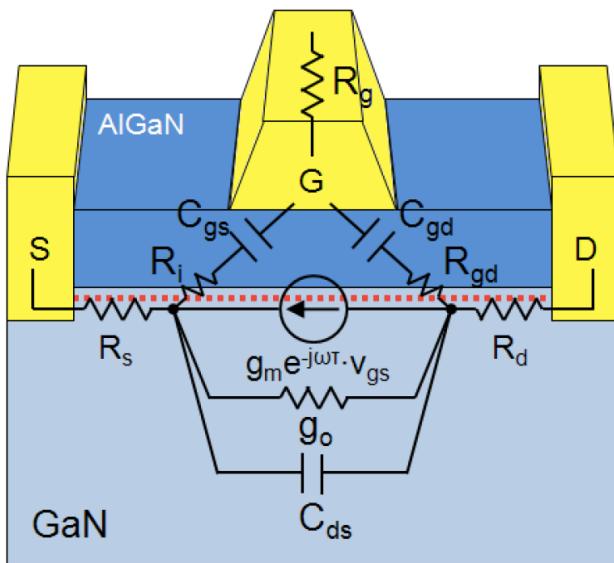


$$g_m = \frac{dI_{DS}}{dV_{GS}} \Big|_{V_{DS}=\text{const.}}$$

$$g_o = \frac{dI_{DS}}{dV_{DS}} \Big|_{V_{GS}=\text{const.}}$$

When the variation of V_{GS} is too fast, I_{DS} cannot be changed immediately since it takes time to charge or discharge C_g (tau is the gm delay)

$$g_m(\omega) = g_m e^{-j\omega\tau}$$



At the current-gain cutoff frequency f_T , the magnitude of current gain equals unity ($|h_{21}| = |i_2/i_1| = 1$) with the output short-circuited

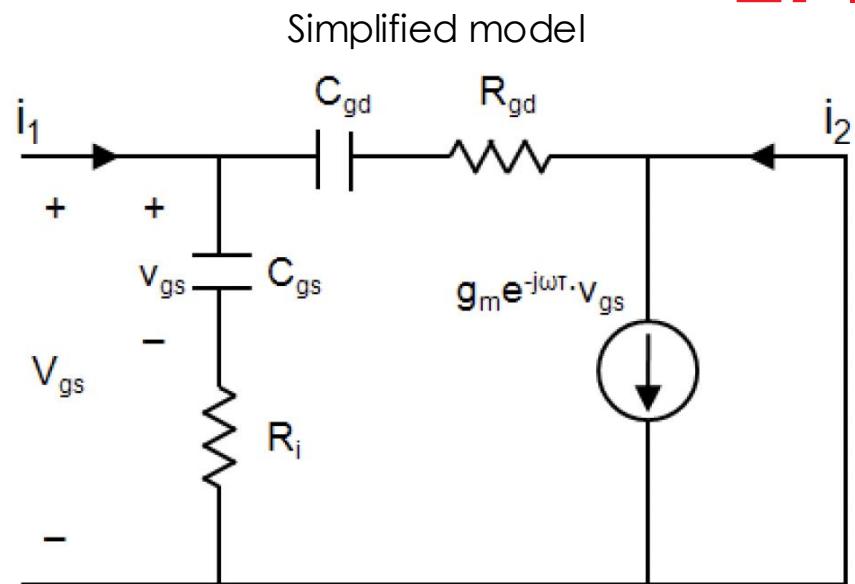
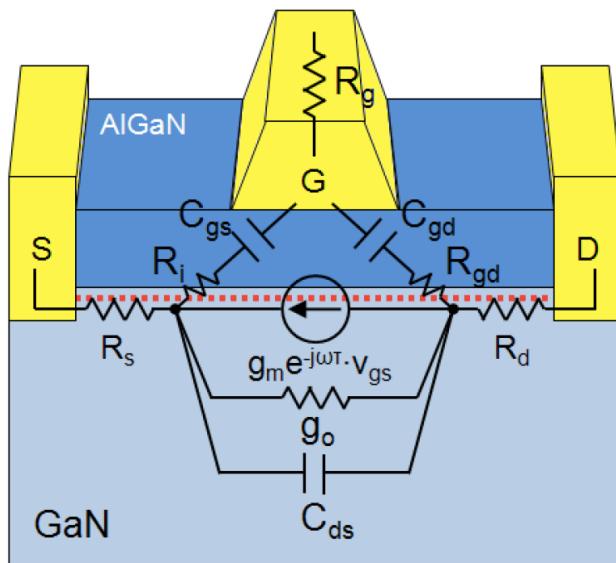
$$A_I|_{r_L=0} = \left. \frac{I_d}{I_g} \right|_{r_L=0} \rightarrow A_I(f_T)|_{r_L=0} = 1 \rightarrow$$

$$i_1 = \frac{V_{gs}}{\frac{1}{j\omega C_{gs}} + R_i} + \frac{V_{gs}}{\frac{1}{j\omega C_{gd}} + R_{gd}}$$

$$i_2 = g_m e^{-j\omega\tau} V_{gs} = g_m e^{-j\omega\tau} \frac{\frac{1}{j\omega C_{gs}}}{\frac{1}{j\omega C_{gs}} + R_i} V_{gs}$$

$$|h_{21}| = \left| \frac{i_2}{i_1} \right| = \left| \frac{(1 + j\omega R_{gd} C_{gd}) g_m e^{-j\omega\tau}}{j\omega(C_{gs} + C_{gd}) - \omega^2 C_{gs} C_{gd} (R_i + R_{gd})} \right| \cong \frac{g_m}{2\pi f (C_{gs} + C_{gd})}$$

term $\omega R_{gd} C_{gd}$ is typically much less than unity and $\omega(C_{gs} + C_{gd}) \gg \omega^2 C_{gs} C_{gd} (R_i + R_{gd})$

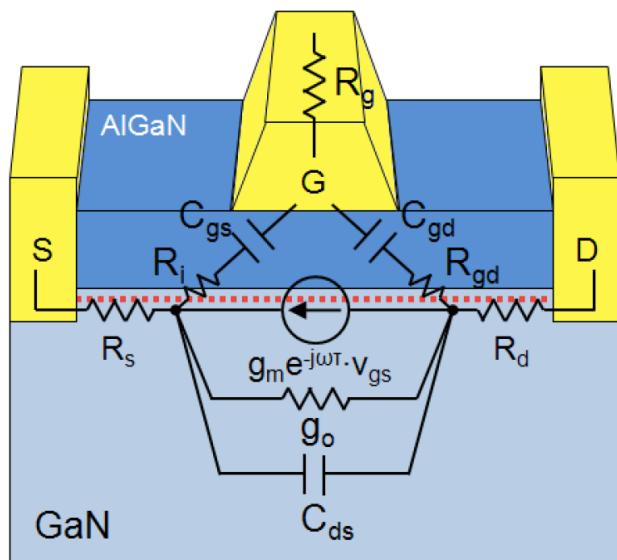


In short gate length devices, an alternative expression for f_T , with a more direct physical meaning, can be written by substituting $g_m = v_{sat}(C_{gs} + C_{gd})/L_g$

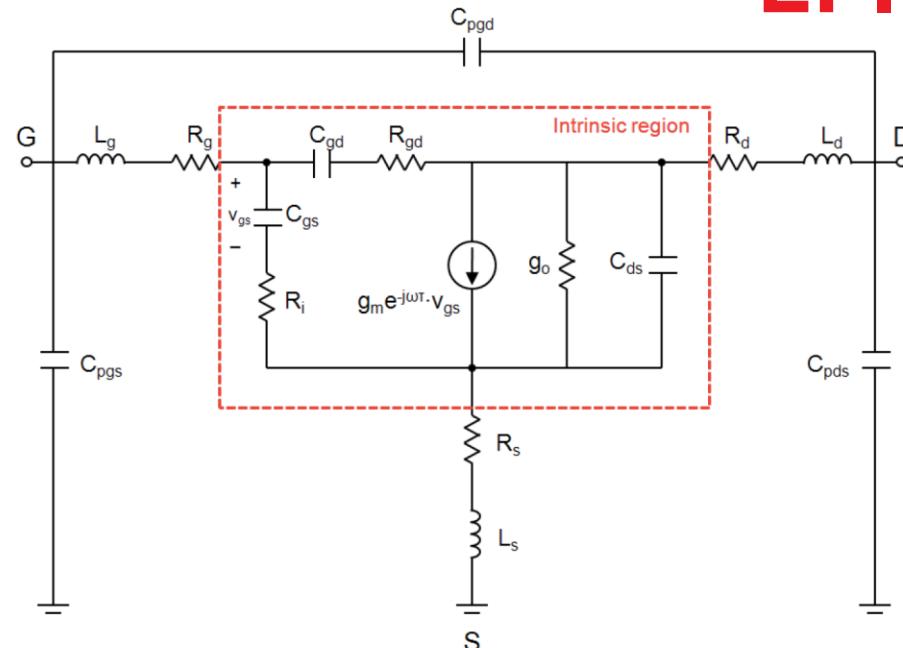
$$f_T = \frac{v_{sat}}{2\pi L_g}$$

Considering extrinsic circuit elements such as R_s , R_d , and g_o :

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})(1 + (R_s + R_d)g_o) + g_m C_{gd}(R_s + R_d)}$$



W. Chung, MIT thesis, 2011



f_T is the frequency at which the magnitude of short-circuit current gain equals unity (or 0 dB)

- f_T is the frequency at which A_I goes to unity when the output is shorted to the ground

$$A_I|_{r_L=0} = \frac{I_d}{I_g} \Big|_{r_L=0} \rightarrow A_I(f_T)|_{r_L=0} = 1 \rightarrow f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})(1 + (R_s + R_d)g_o) + g_m C_{gd}(R_s + R_d)}$$

f_{max} is the frequency at which the unilateral power gain equals unity (or 0 dB)

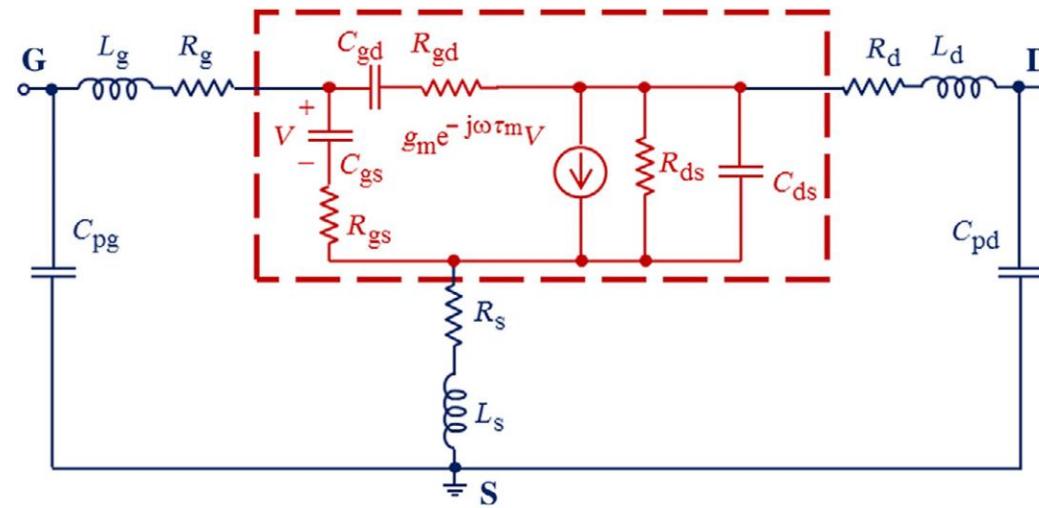
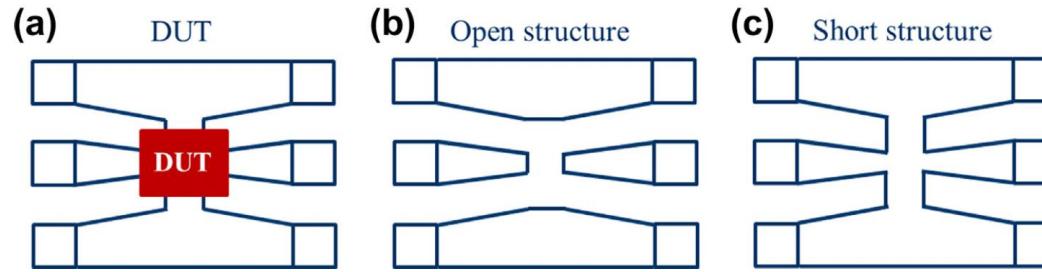
- f_{max} is the frequency at which A_P goes to unity when the input/source and output/load are matched conjugately

$$A_P(f_{max}) \Big|_{z_s=z_{in}^* \text{ and } z_L=z_{out}^*} = 1 \rightarrow f_{max} \cong \frac{f_T}{2\sqrt{(R_i + R_s + R_g)g_o + (2\pi f_T)R_g C_{gd}}}$$

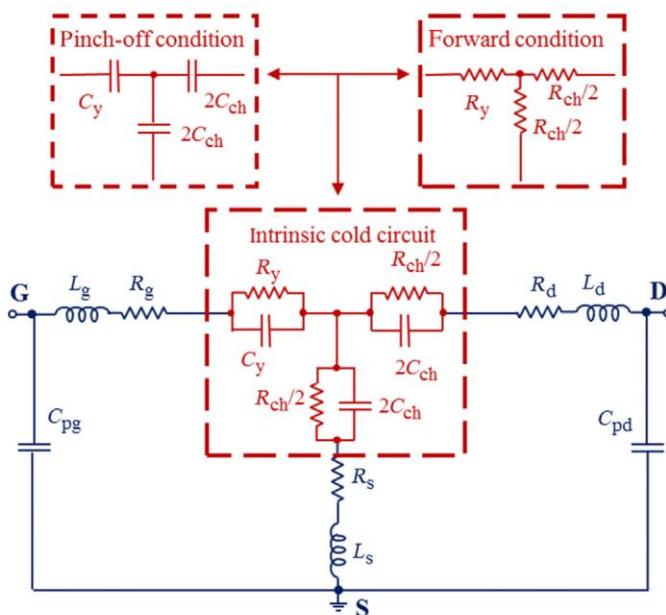
Optimization of f_{max} relies on the maximizing f_T and reduction of R_i , R_s , R_g , C_{gd} , and g_o

Measuring high frequency devices

De-embedding the pads to retrieve the intrinsic device components



Different bias conditions can be used to reveal different circuit elements



$$Y_{11} = \frac{1}{R_{gs} + \frac{1}{j\omega C_{gs}}} + \frac{1}{R_{gd} + \frac{1}{j\omega C_{gd}}} \\ = \frac{\omega^2 R_{gs} C_{gs}^2}{1 + \omega^2 R_{gs}^2 C_{gs}^2} + \frac{\omega^2 R_{gd} C_{gd}^2}{1 + \omega^2 R_{gd}^2 C_{gd}^2} + j\omega \left(\frac{C_{gs}}{1 + \omega^2 R_{gs}^2 C_{gs}^2} + \frac{C_{gd}}{1 + \omega^2 R_{gd}^2 C_{gd}^2} \right)$$

$$Y_{21} = \frac{\frac{g_m e^{-j\omega\tau_m}}{j\omega C_{gs}}}{R_{gs} + \frac{1}{j\omega C_{gs}}} - \frac{1}{R_{gd} + \frac{1}{j\omega C_{gd}}} = \frac{g_m [\cos(\omega\tau_m) - \sin(\omega\tau_m)\omega R_{gs} C_{gs}]}{1 + \omega^2 R_{gs}^2 C_{gs}^2} +$$

$$- \frac{\omega^2 R_{gd} C_{gd}^2}{1 + \omega^2 R_{gd}^2 C_{gd}^2} - j \left\{ \frac{g_m [\cos(\omega\tau_m)\omega R_{gs} C_{gs} + \sin(\omega\tau_m)]}{1 + \omega^2 R_{gs}^2 C_{gs}^2} + \frac{\omega C_{gd}}{1 + \omega^2 R_{gd}^2 C_{gd}^2} \right\}$$

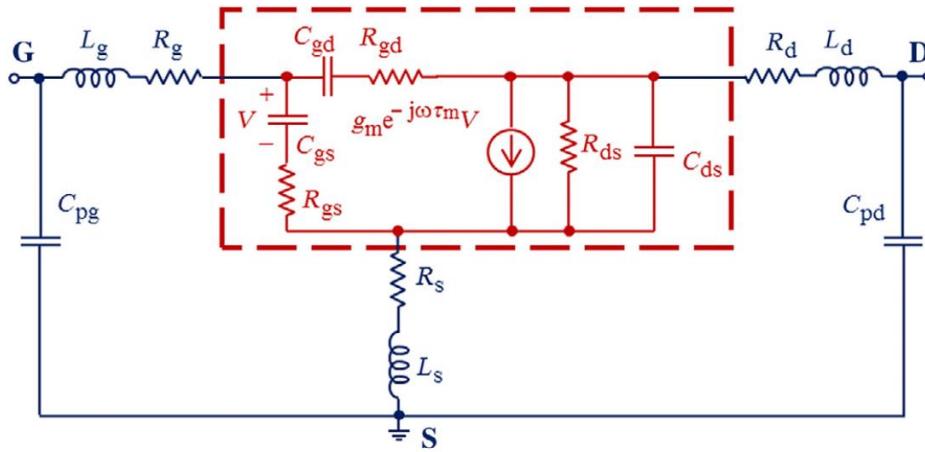
$$Y_{12} = - \frac{1}{R_{gd} + \frac{1}{j\omega C_{gd}}} \\ = - \frac{\omega^2 R_{gd} C_{gd}^2}{1 + \omega^2 R_{gd}^2 C_{gd}^2} - \frac{j\omega C_{gd}}{1 + \omega^2 R_{gd}^2 C_{gd}^2}$$

$$Y_{22} = g_{ds} + j\omega C_{ds} + \frac{1}{R_{gd} + \frac{1}{j\omega C_{gd}}}$$

$$= g_{ds} + \frac{\omega^2 R_{gd} C_{gd}^2}{1 + \omega^2 R_{gd}^2 C_{gd}^2} + j\omega \left(C_{ds} + \frac{C_{gd}}{1 + \omega^2 R_{gd}^2 C_{gd}^2} \right)$$

Measuring high frequency devices

All small signal intrinsic elements can be retrieved



$$R_{gd} = -\text{Re}\left(\frac{1}{Y_{12}}\right)$$

$$C_{gd} = \frac{1}{\omega \text{Im}\left(\frac{1}{Y_{12}}\right)}$$

$$R_{gs} = \text{Re}\left(\frac{1}{Y_{11} + Y_{12}}\right)$$

$$C_{gs} = -\frac{1}{\omega \text{Im}\left(\frac{1}{Y_{11} + Y_{12}}\right)}$$

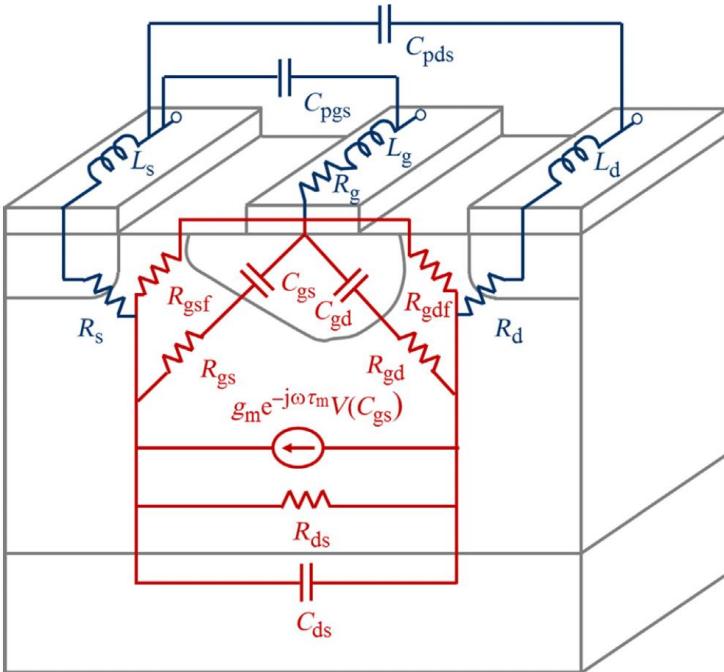
$$R_{ds} = \frac{1}{\text{Re}(Y_{22} + Y_{12})}$$

$$C_{ds} = \frac{\text{Im}(Y_{22} + Y_{12})}{\omega}$$

$$g_m = \frac{|(Y_{11} + Y_{12})(Y_{21} - Y_{12})|}{\text{Im}(Y_{11} + Y_{12})}$$

$$\tau_m = -\frac{1}{\omega} \text{phase} \left\{ (Y_{21} - Y_{12}) \left[1 + j \frac{\text{Re}(Y_{11} + Y_{12})}{\text{Im}(Y_{11} + Y_{12})} \right] \right\}$$

Y parameters (admittance matrix) are connected to physical device parameters, but it is difficult to measure voltages and currents, and realize short-circuit terminations in microwave ranges



$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$$

$$i_1 = y_{11}v_1 + y_{12}v_2 \quad i_2 = y_{21}v_1 + y_{22}v_2$$

$$y_{11} = \frac{i_1}{v_1} \Big|_{v_2=0} \quad y_{12} = \frac{i_1}{v_2} \Big|_{v_1=0} \quad y_{21} = \frac{i_2}{v_1} \Big|_{v_2=0} \quad y_{22} = \frac{i_2}{v_2} \Big|_{v_1=0}$$

S parameters can be measured with VNAs:

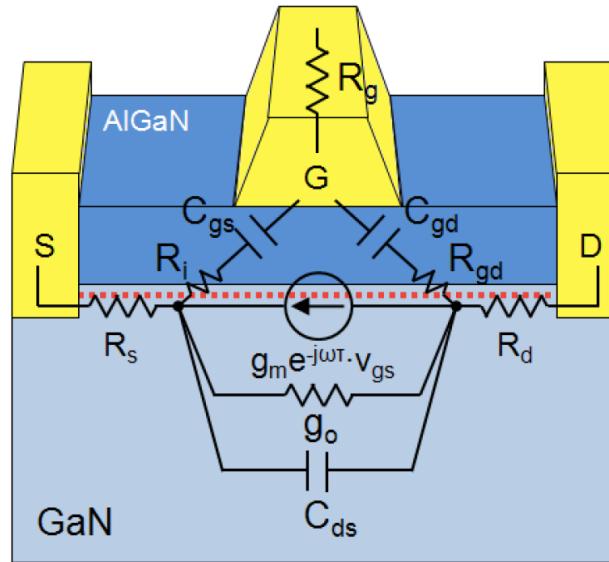
$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

$$b_1 = s_{11}a_1 + s_{12}a_2 \quad b_2 = s_{21}a_1 + s_{22}a_2$$

$$s_{11} = \frac{b_1}{a_1} \Big|_{\text{output match}} \quad s_{12} = \frac{b_1}{a_2} \Big|_{\text{input match}} \quad s_{21} = \frac{b_2}{a_1} \Big|_{\text{output match}} \quad s_{22} = \frac{b_2}{a_2} \Big|_{\text{input match}}$$

The small-signal implies that the magnitude of the signal voltage is $\sim kT / q$ (~ 26 mV at $T = 300$ K):
 Nonlinear characteristics of field-effect transistors can be linearized

GaN RF transistors



Scaling	Material properties	Advantage
Vertical scaling	<ul style="list-style-type: none"> High DoS in GaN ($5 \times$ InGaAs) Polarization doping High potential barrier of AlGaN 	<ul style="list-style-type: none"> High vertical scalability Thin top barrier w/ high n_s Low gate leakage
Lateral scaling	<ul style="list-style-type: none"> High peak saturation velocity High breakdown field 	<ul style="list-style-type: none"> High $JFOM$ ($JFOM = f_T \times BV$)
Parasitic reduction	<ul style="list-style-type: none"> High n_s ($1-2 \times 10^{13} \text{ cm}^{-2}$) High μ ($1500 \text{ cm}^2/\text{V}\cdot\text{s}$) 	<ul style="list-style-type: none"> Low parasitic resistance ($\sigma = n_s \cdot q \cdot \mu$)

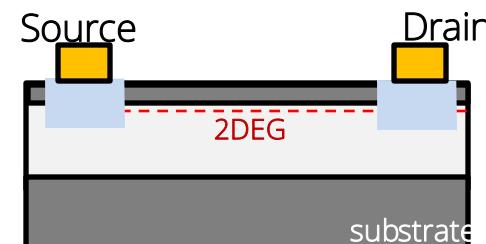
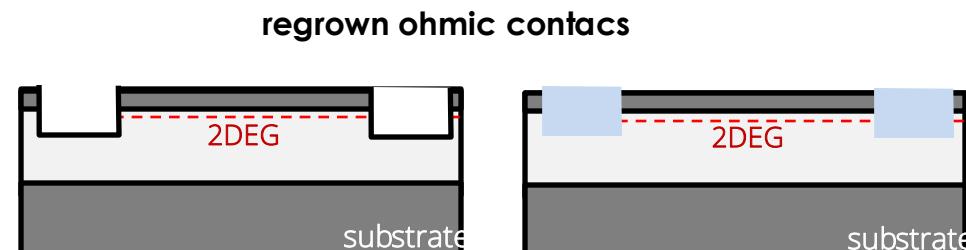
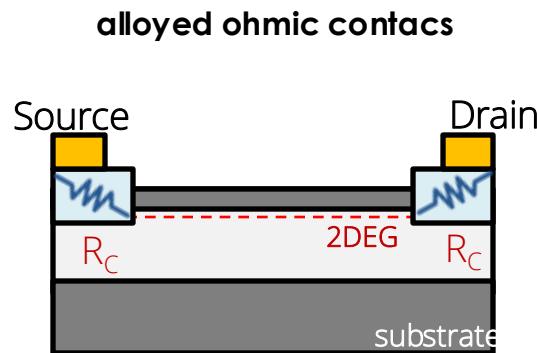
Effect of contact resistance

Contact resistances:

Important RC charging times are reduced by minimizing source and drain resistances and parasitic capacitances.

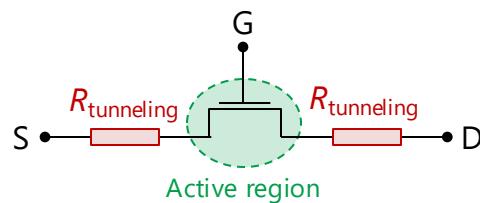
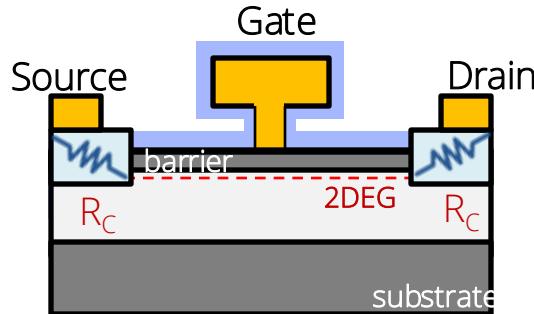
Conventional alloyed ohmic contacts: typically exhibit a high contact resistance of $>0.4 \text{ ohm} \cdot \text{mm}$ due to high potential barrier of AlGaN, limiting resistance scaling.

Regrown n⁺GaN contacts: allows direct contact of n⁺-GaN to 2DEG and obtains an extremely low interface resistance of $0.026 \text{ } \cdot \text{mm}$ because of high n_s in GaN HEMT structures [2]. A combination of high n_s and high mobility (μ) also results in a low 2DEG sheet resistance (typically, 300–400 /sq.) that is comparable to InGaAs HEMTs, reducing the parasitic resistance in access regions.



Effect of contact resistance

Contact resistance is not scalable



$$R_{\text{tunneling}}^{\text{quantum-limit}} \approx 30 \Omega \cdot \mu\text{m}$$

Resistance of a 100-nm-long semiconductor channel !

Quantum limit

$$R_q = \pi h / (4q^2 k_F)$$

Electron injection through metal-semiconductor contacts limits their ON-state conductance

IEEE ELECTRON DEVICE LETTERS, VOL. 36, NO. 6, JUNE 2015

Ultrahigh-Speed GaN High-Electron-Mobility Transistors With f_T/f_{max} of 454/444 GHz

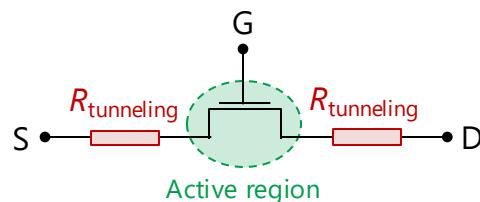
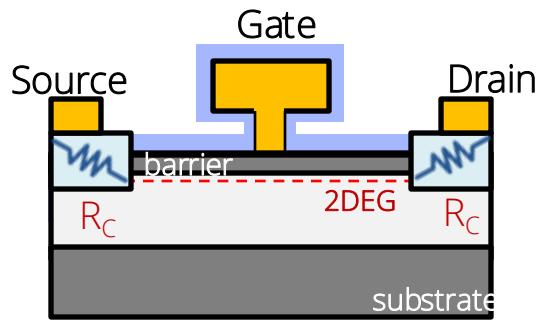
Yan Tang, Keisuke Shinohara, *Senior Member, IEEE*, Dean Regan, Andrea Corrion, *Member, IEEE*, David Brown, *Member, IEEE*, Joel Wong, Adele Schmitz, Helen Fung, Samuel Kim, and Miroslav Micovic, *Member, IEEE*

R_{channel}	R_{source}	R_{drain}
$40 \Omega \cdot \mu\text{m}$	$50 \Omega \cdot \mu\text{m}$	$120 \Omega \cdot \mu\text{m}$



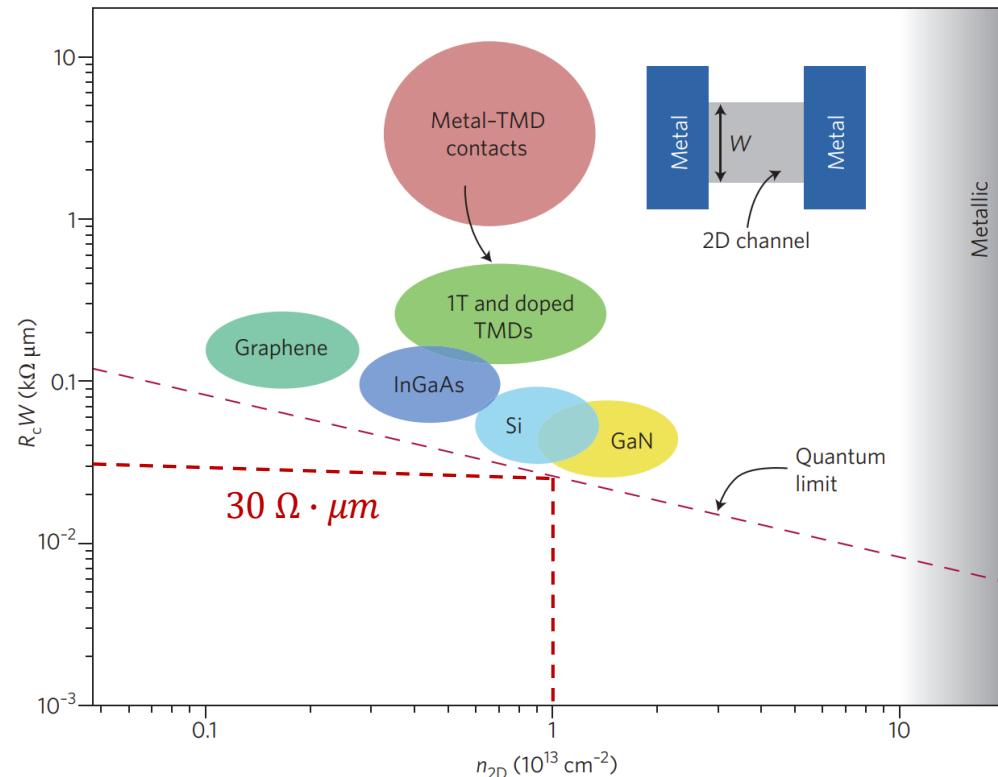
Effect of contact resistance

Contact resistance is not scalable



$$R_{\text{tunneling}}^{\text{quantum-limit}} \cong 30 \Omega \cdot \mu\text{m}$$

Resistance of a 100-nm-long semiconductor channel !



Quantum limit

$$R_q = \pi h / (4q^2 k_F)$$

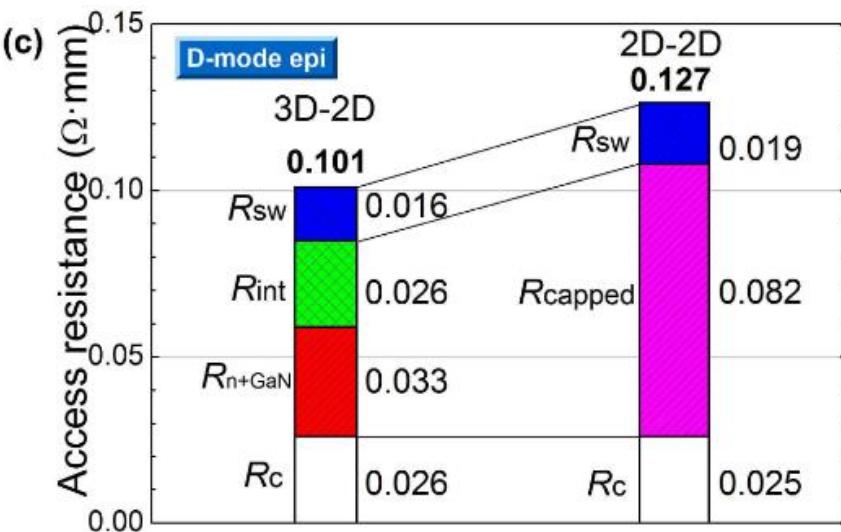
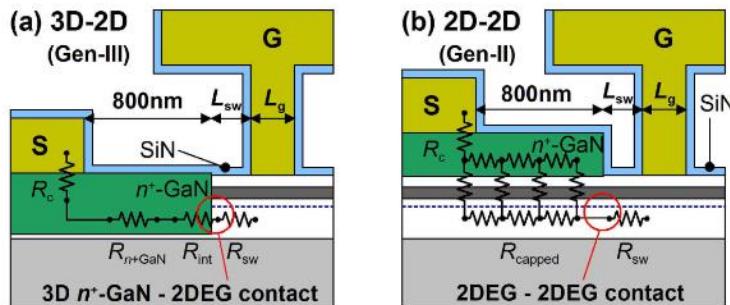
Electron injection through metal-semiconductor contacts limits their ON-state conductance

Contact resistances:

Important RC charging times are reduced by minimizing source and drain resistances and parasitic capacitances.

Conventional alloyed ohmic contacts: typically exhibit a high contact resistance of $>0.4 \text{ ohm}\cdot\text{mm}$ due to high potential barrier of AlGaN, limiting resistance scaling.

Regrown n⁺GaN contacts: allows direct contact of n⁺-GaN to 2DEG and obtains an extremely low interface resistance of $0.026 \text{ }\cdot \text{ mm}$ because of high n_s in GaN HEMT structures [2]. A combination of high n_s and high mobility (μ) also results in a low 2DEG sheet resistance (typically, 300–400 /sq.) that is comparable to InGaAs HEMTs, reducing the parasitic resistance in access regions.

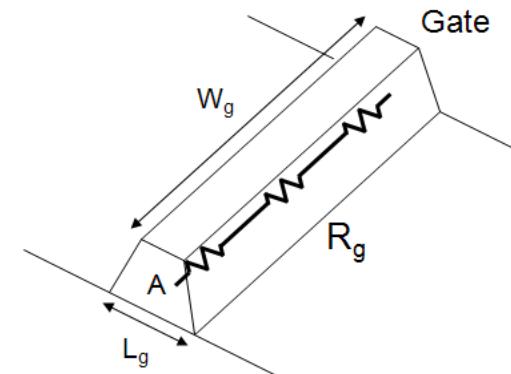
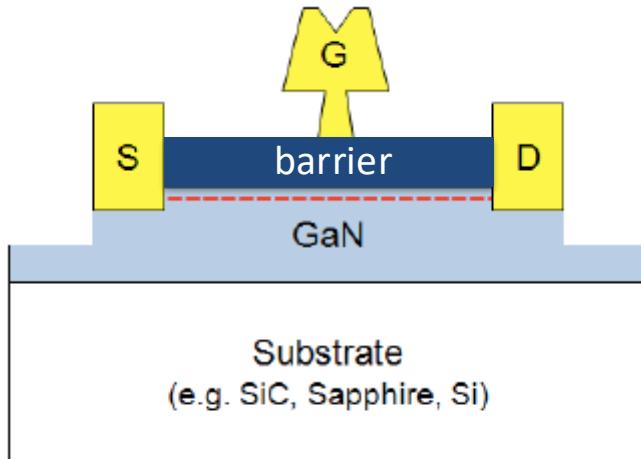


Effect of gate shape

Gate contacts: one of the most important steps for RF

- Gate modulation (g_m)
- Gate capacitances by the gate contact (C_{gs} and C_{gd})
- Gate resistance R_g to improve f_{max}

T gates



$$\text{Gate resistance: } R_g \propto \rho W / A$$

Small R_g requires large L_g

$$\text{Gate capacitance: } C_{gd} = \frac{2\epsilon W_g}{1 + \frac{2X_{dep}}{L_g}}$$

Small C requires small L_g

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})(1 + (R_s + R_d)g_o) + g_m C_{gd}(R_s + R_d)}$$



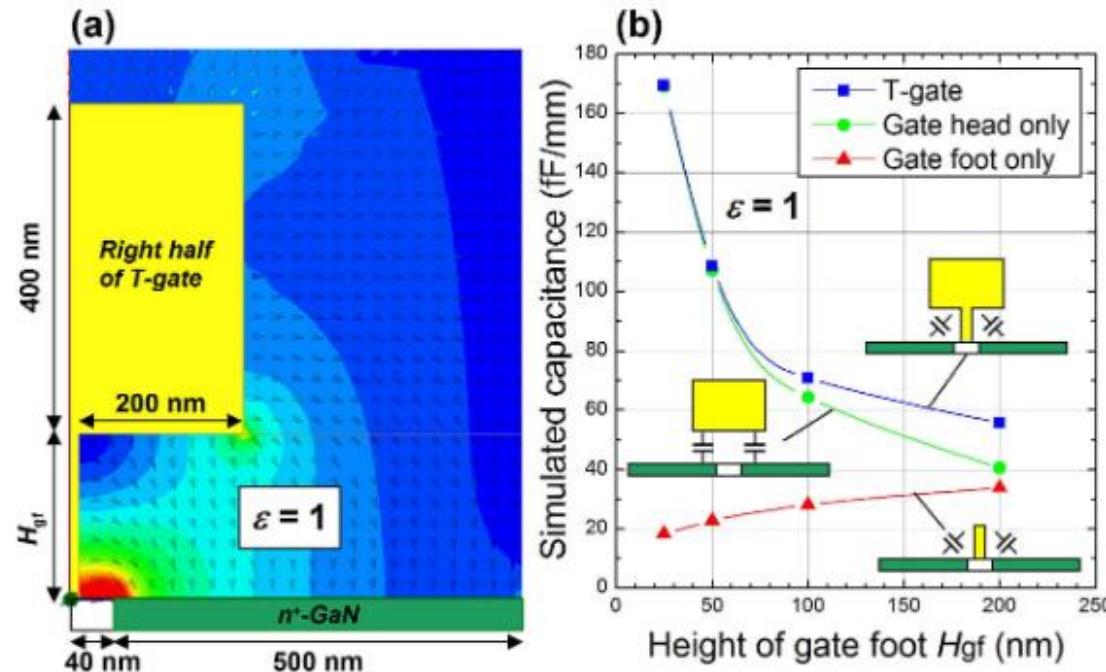
$$f_{max} \cong \frac{f_T}{2\sqrt{(R_i + R_s + R_g)g_o + (2\pi f_T)R_g C_{gd}}}$$



Gate contacts: one of the most important steps for RF

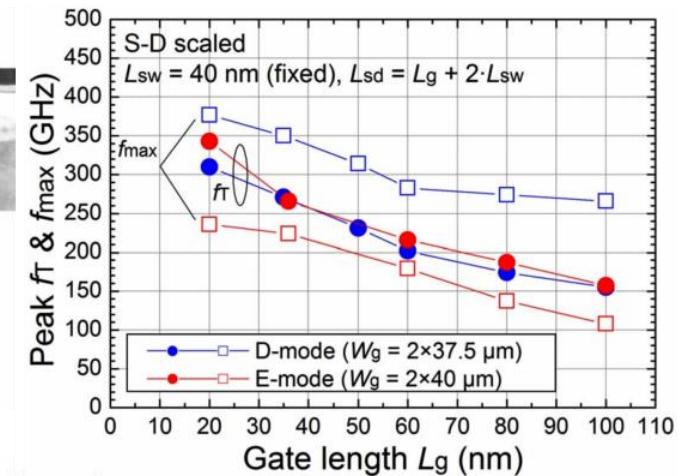
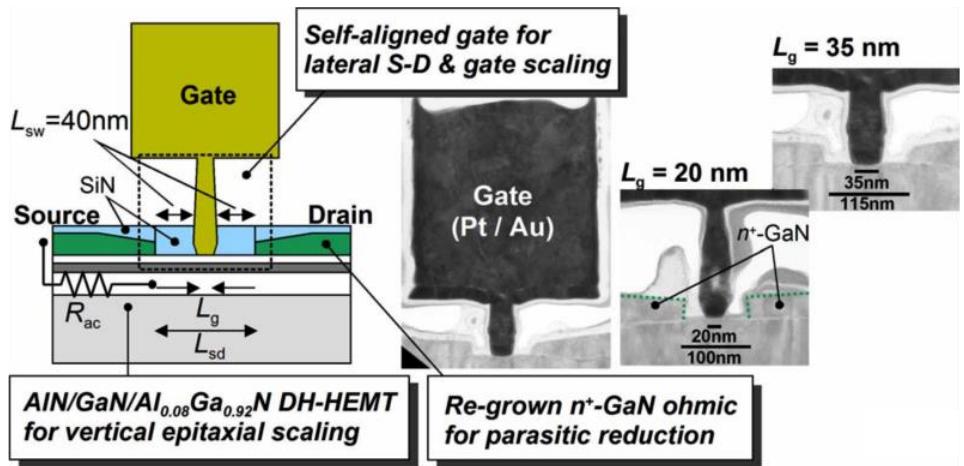
- Gate modulation (g_m)
- Gate capacitances by the gate contact (C_{gs} and C_{gd})
- Gate resistance R_g to improve f_{max}

T gates



For $H_{gf} < 100$ nm, C_p is mostly determined by the high capacitance associated with the gate head. At $H_{gf} = 200$ nm, C_p 's arising from the gate-head and the gatefoot become comparable, and a further increase in H_{gf} does not significantly reduce the total C_p .

Effect of gate shape



20-nm gate AlN/GaN/AlGaN double heterojunction HEMTs: $f_T/f_{MAX} = 310/364$ GHz

HRL laboratories: K.Shinohara et al. , IEDM 11-456 (2011).

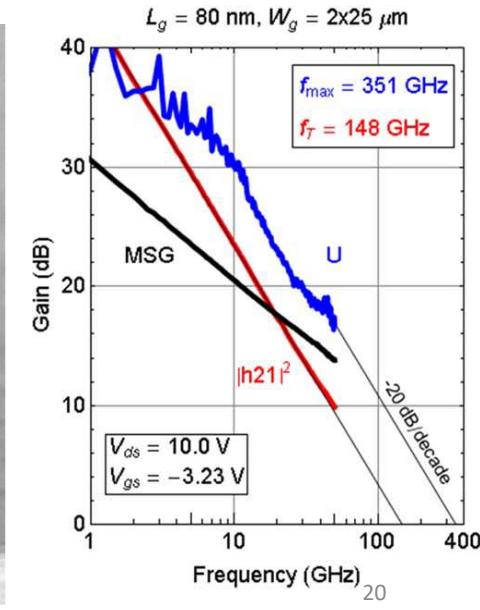
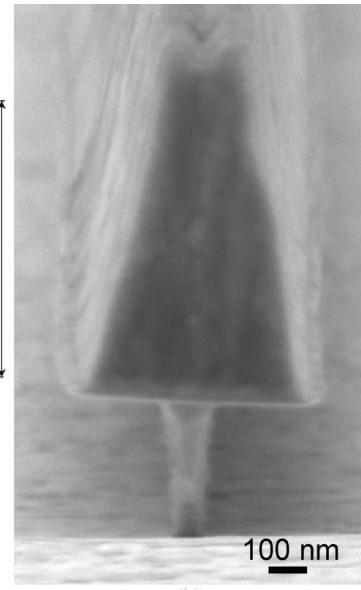
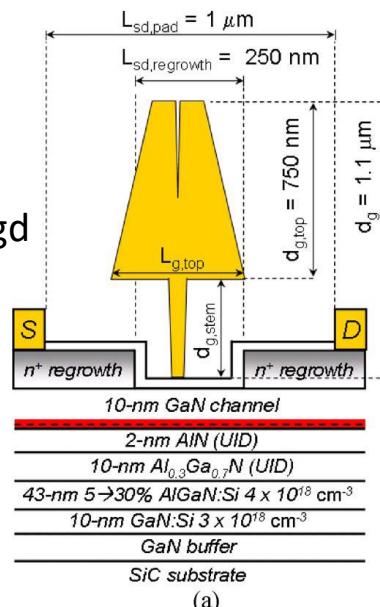
Gates:

- 80-nm-long 1.1-μm-tall

- 370-nm-tall stem

simultaneously minimize R_g and C_{gd}

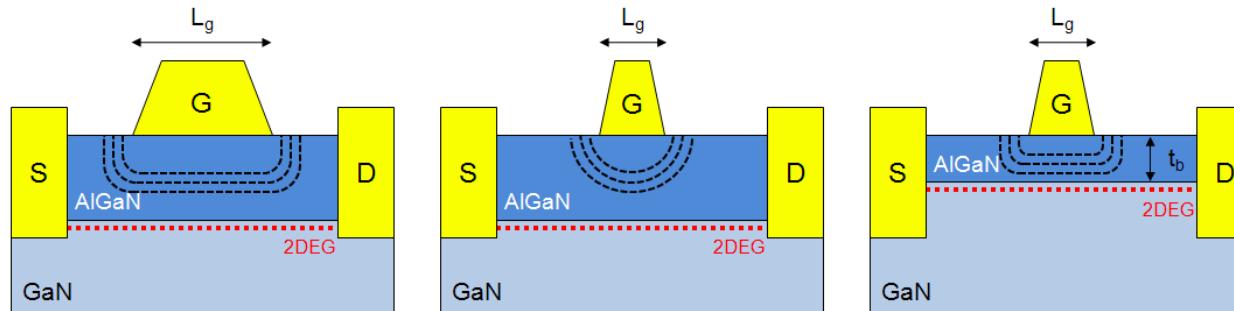
$F_{max} = 351$ GHz



To obtain improved HEMT frequency response by scaling, the electron transit time is reduced by laterally scaling the gate length (L_g). Accordingly, the thicknesses of HEMT epitaxial layers must be reduced to prevent **shortchannel effect** — degraded drain current modulation by the gate voltage seen in very short gate HEMTs — which causes a negative threshold voltage (V_{th}) shift and an increased draininduced barrier lowering (DIBL).

Scaling effects:

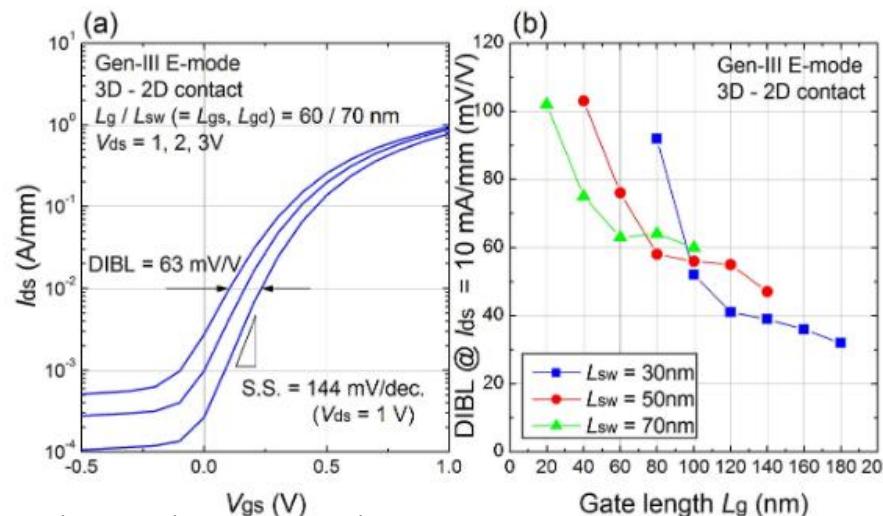
Field distribution in the channel becomes two-dimensional with both E_x and E_y : Short channel effects



Barrier needs to be scaled accordingly $t_b \ll L_g$, typically, $L_g/t_b > 5...$ but carrier density is reduced

For example: 20-nm L_g , the top barrier thickness needs to be reduced to 4 nm

Y Cordier, T Fujishima, B Lu, E Matioli, T Palacios - III-Nitride Semiconductors and their Modern Devices, 2013

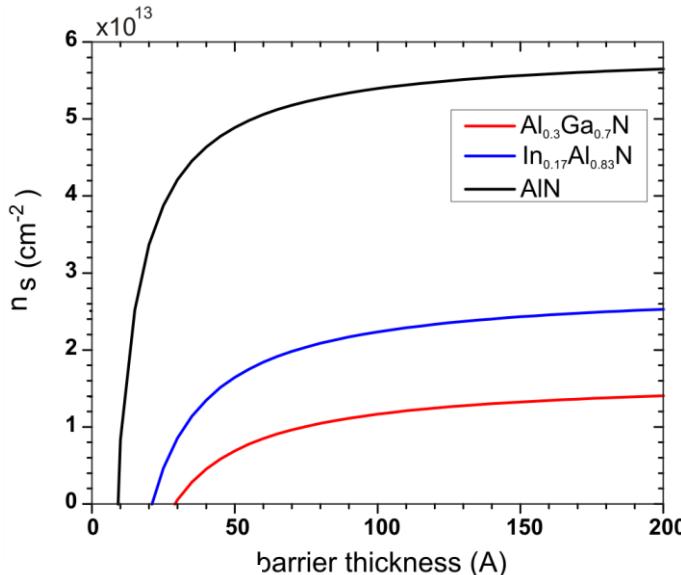


Effect of barrier material

Barrier materials with **large polarization discontinuities** allow:

- reduced barrier thicknesses
- improved gate control over electrons in the channel
- improvement in short channel effects:

InAlN, AlN, AlInGaN, etc



Y Cordier, T Fujishima, B Lu, E Matioli, T Palacios - III-Nitride Semiconductors and their Modern Devices, 2013

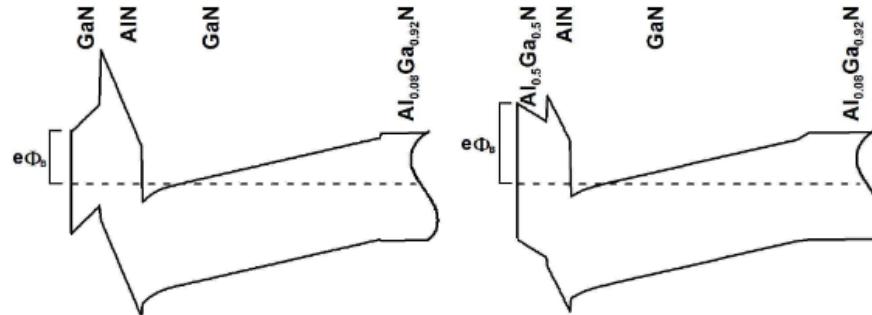
Use of back barriers:

(a) D-mode epi

GaN cap	2.5 nm
AlN top barrier	3.5 nm
GaN channel	20 nm
$\text{Al}_{0.08}\text{Ga}_{0.92}\text{N}$ back barrier	
S.I. SiC sub.	

(b) E-mode epi

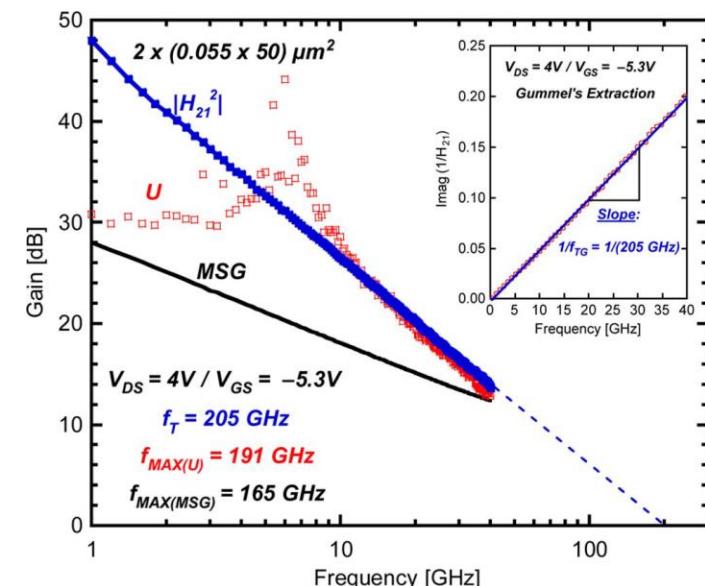
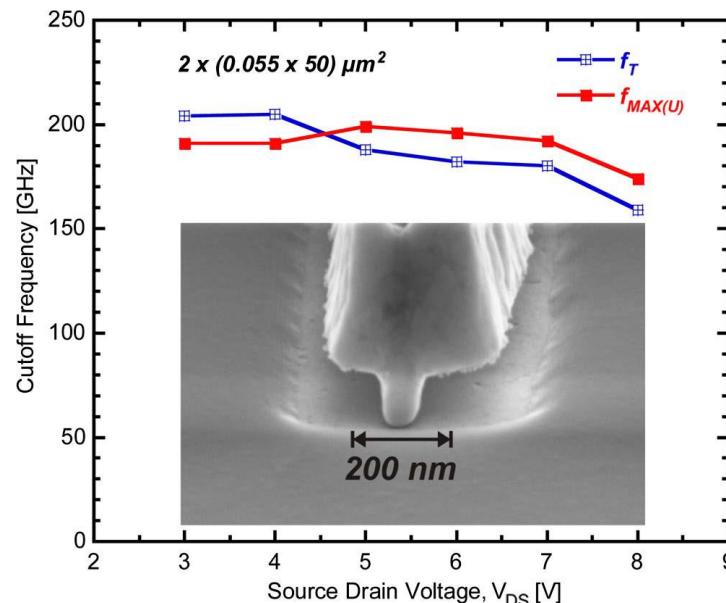
$\text{Al}_{0.5}\text{Ga}_{0.5}\text{N}$ cap	2.5 nm
AlN top barrier	2.0 nm
GaN channel	20 nm
$\text{Al}_{0.08}\text{Ga}_{0.92}\text{N}$ back barrier	
S.I. SiC sub.	



Effect of barrier material

AlInN/GaN

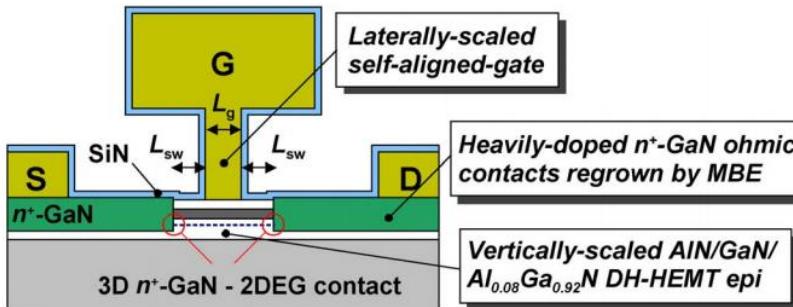
- Al_{0.83}In_{0.17}N is lattice-matched to GaN
- Polarization-field discontinuity $\Delta P_0 = 2.73 \times 10^{13} \text{ ecm}^{-2}$ solely due to spontaneous polarization
in contrast to Al_{0.2}Ga_{0.8}N/GaN ($\Delta P_0 = 1.18 \times 10^{13} \text{ ecm}^{-2}$) from spontaneous and piezoelectric polarization
- First proposed in J. Kuzmík, IEEE Electron Device Lett., vol.22, no.11, p.510 (2001))



- 10-nm nearly lattice-matched Al_{0.86}In_{0.14}N barrier
- channel electron sheet density of $2.4 \times 10^{13} \text{ cm}^{-2}$
- mobility $\mu = 1300 \text{ cm}^2/\text{Vs}$
- gate length = 55 nm and f_T/f_{MAX} of 205/191 GHz

Effect of barrier material

AlN/GaN

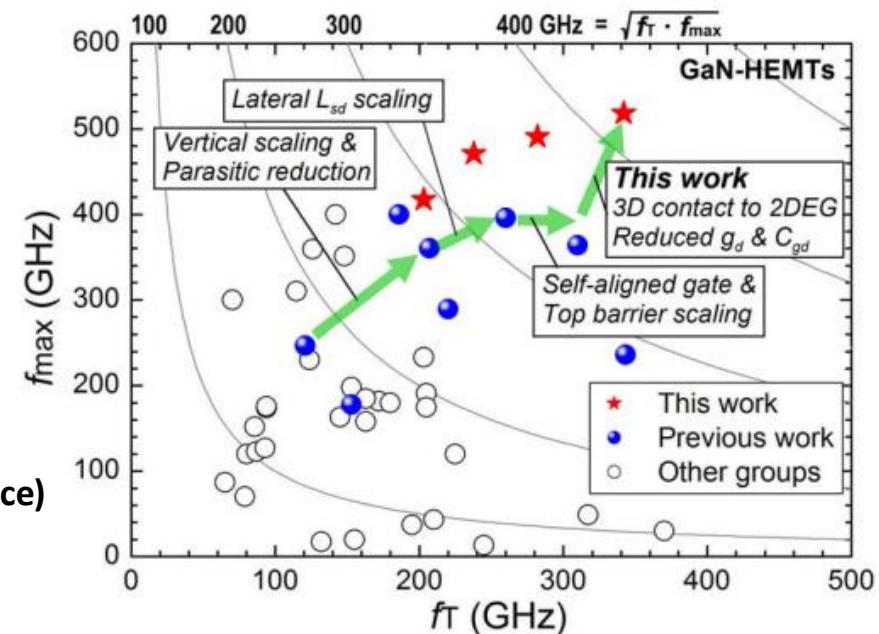


IEEE ELECTRON DEVICE LETTERS, VOL. 36, NO. 6, JUNE 2015

Ultrahigh-Speed GaN High-Electron-Mobility Transistors With f_T/f_{\max} of 454/444 GHz

Yan Tang, Keisuke Shinohara, Senior Member, IEEE, Dean Regan, Andrea Corrion, Member, IEEE, David Brown, Member, IEEE, Joel Wong, Adele Schmitz, Helen Fung, Samuel Kim, and Miroslav Micovic, Member, IEEE

- Barrier thickness: 3.5 nm
- $n_s = 1.5 \times 10^{13} \text{ cm}^{-2}$
- **mobility (μ) of $1100 \text{ cm}^2/\text{V}\cdot\text{s}$**
- Si-doped n+-GaN ohmic ($7 \times 10^{19} \text{ cm}^{-3}$):
to laterally contact to 2DEG in the GaN channel
- ultra-short gate length of 20nm
- gate-source and gate-drain separation of 70nm
- **f_T / f_{\max} as high up to 454/518GHz (not on the same device)**
- **However, $V_{br} = 10V$**



HRL laboratories:

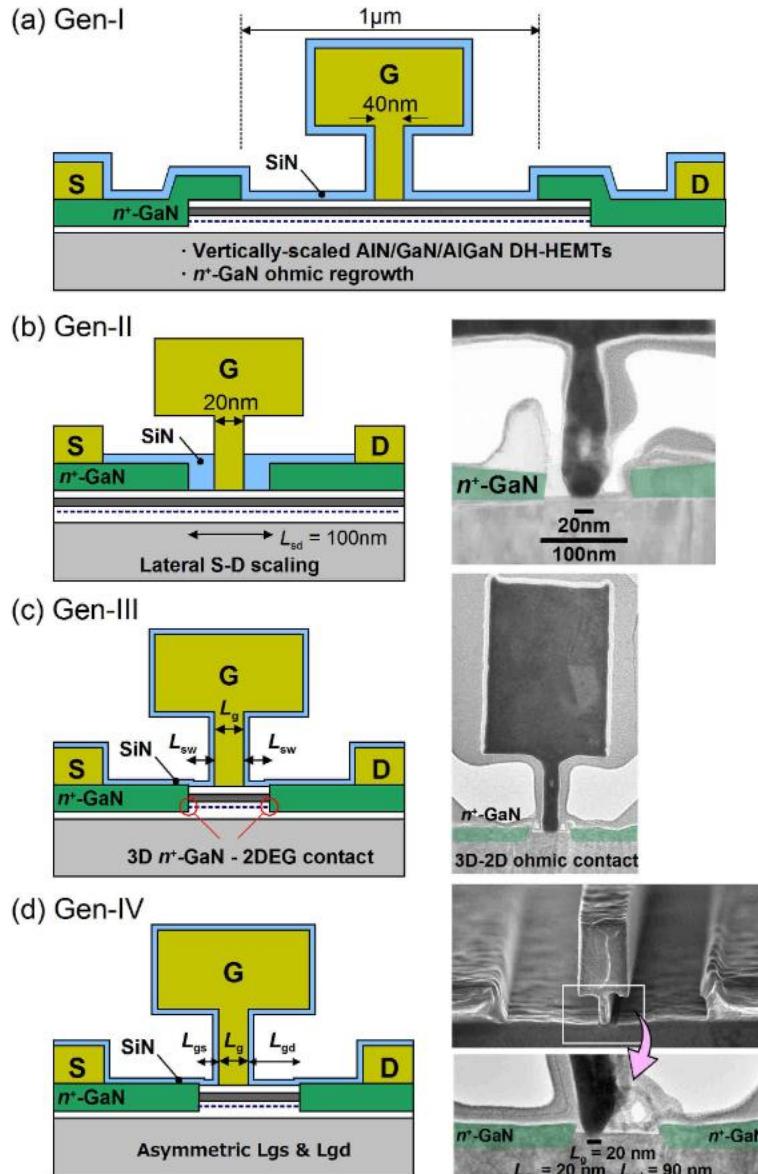
Shinohara et al., IEDM 2011

Shinohara et al., IEEE IEDM, Dec. 2012

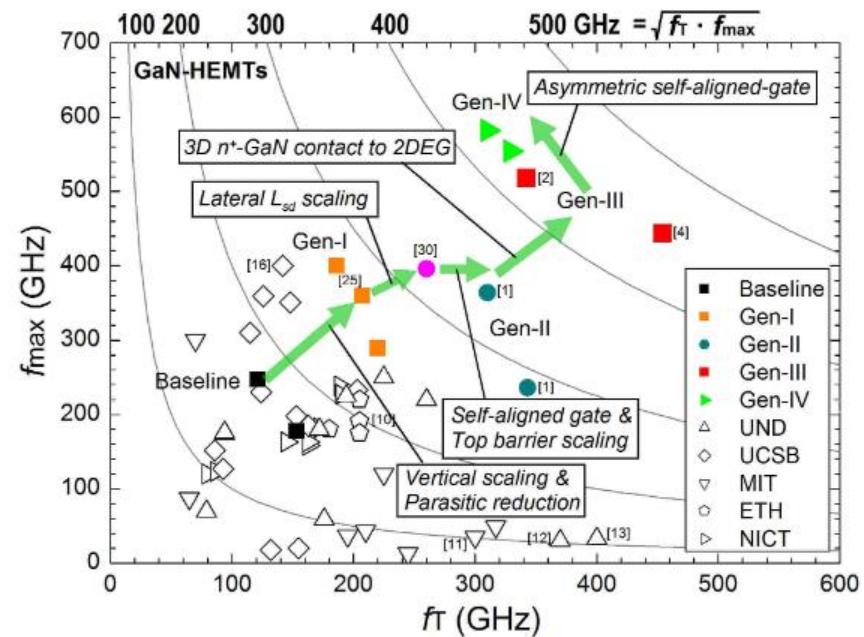
Tang et al., IEEE ELECTRON DEVICE LETTERS, VOL. 36, NO. 6, JUNE 2015

Evolution of several technologies

AlN/GaN



Scaling generation	Specific features
Gen-I	<ul style="list-style-type: none"> Vertically-scaled AlN/GaN/AlGaN DH-HEMT epi structure Low resistance n^+-GaN ohmic regrowth
Gen-II	<ul style="list-style-type: none"> Lateral S-D scaling using self-aligned-gate technology Suppressed drain delay & velocity enhancement
Gen-III	<ul style="list-style-type: none"> Direct contact of 3D n^+-GaN ohmic to 2DEG Reduced R_{on} and enhanced electron supply (J_{dmax}, g_m) E/D-mode integrated DCFL ring oscillators
Gen-IV	<ul style="list-style-type: none"> Asymmetric self-aligned-gate technology Increased BV and reduced short-channel effect ($DIBL$, f_{max}) Low noise characteristics at low power

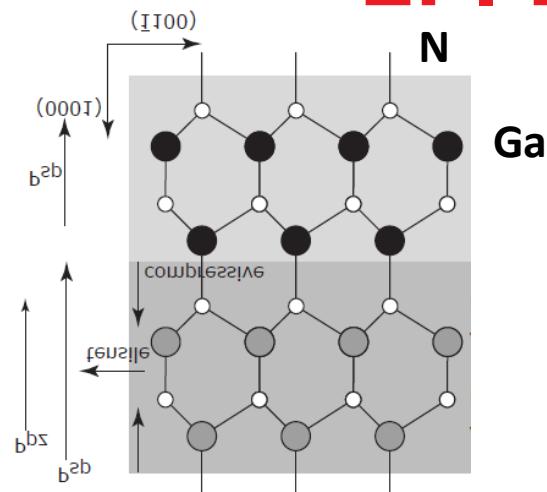


Effect of barrier material

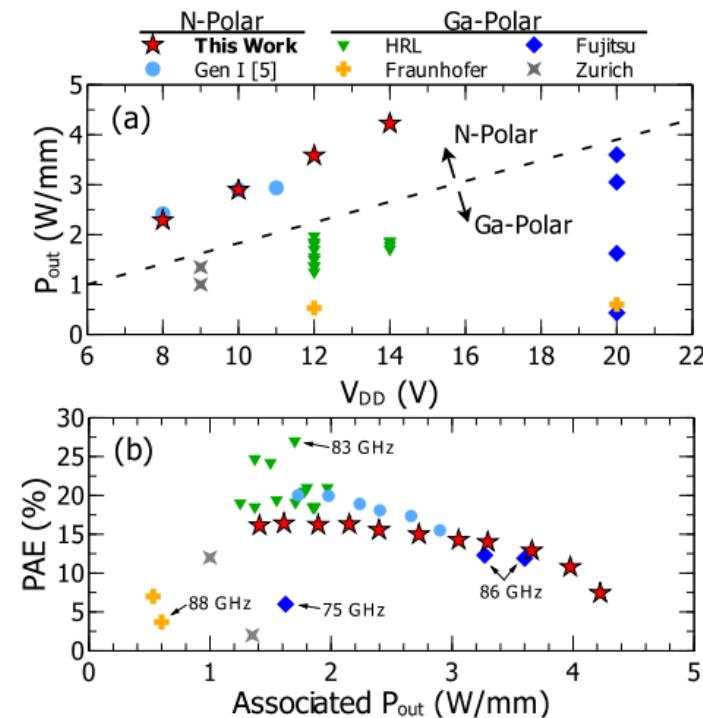
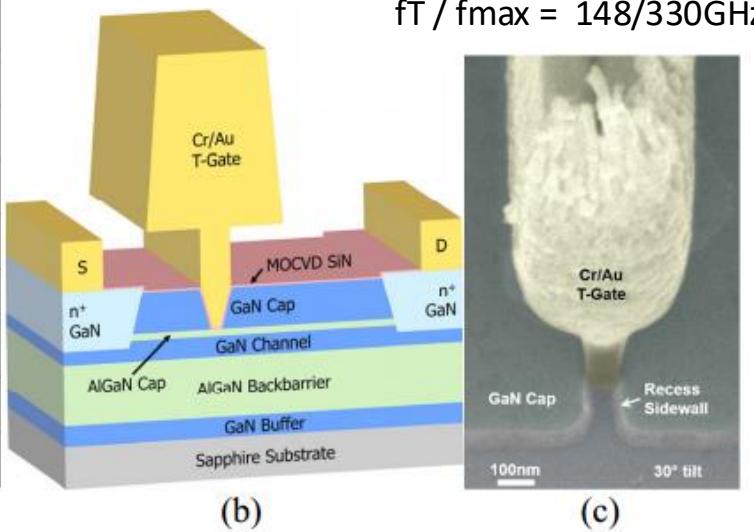
N-polar GaN

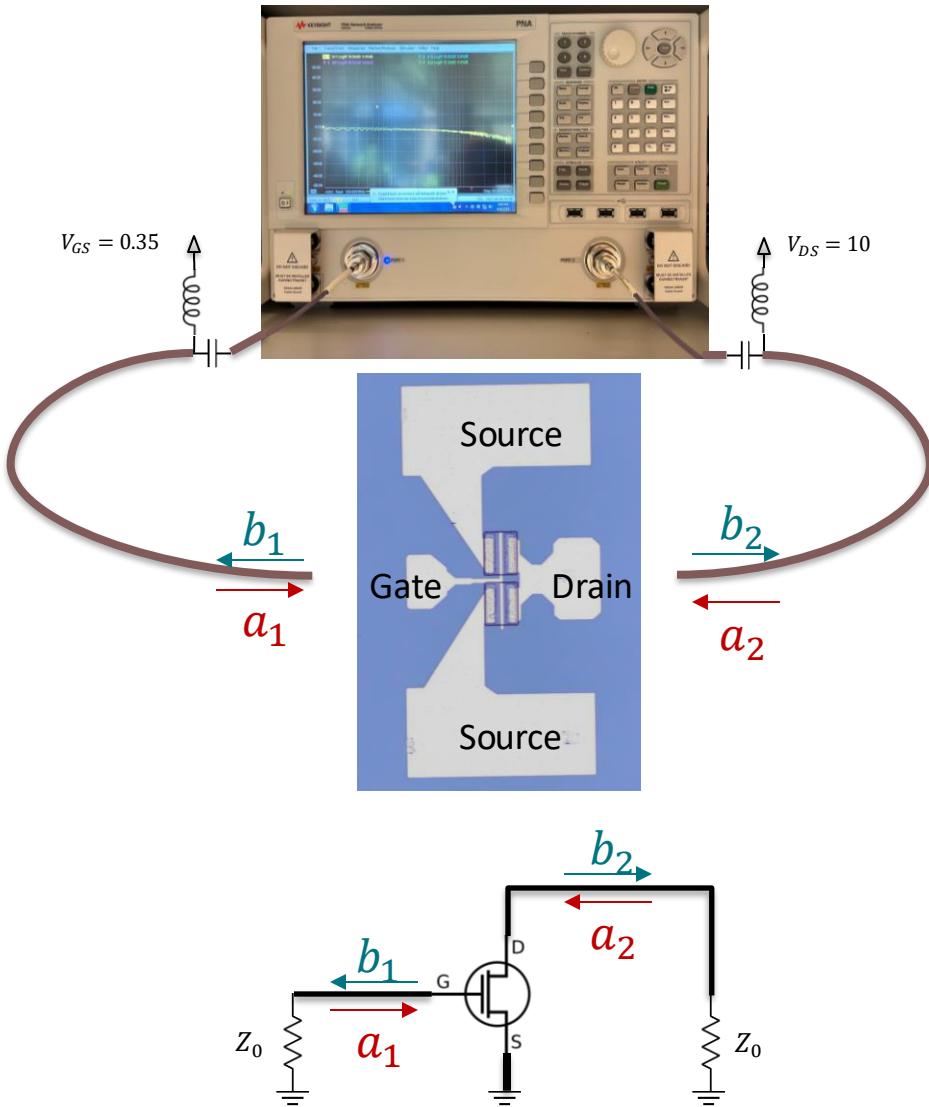
Reversed polarization fields of N-polar GaN/Al(In,Ga)N offers

- improved electron confinement
- flexibility to scale the gate-to-2DEG distance without changing the charge density in the 2DEG.
- Ultra low contact resistance values since the contacts are not made through a high band-gap barrier ($\sim 30 \Omega\text{um}$)
- improved gate-channel distance scalability
- Improved breakdown voltage



22 nm GaN Cap
2.6 nm $\text{Al}_{0.27}\text{Ga}_{0.73}\text{N}$ Cap
10 nm GaN Channel
0.7 nm $\text{Al}_{0.48}\text{Ga}_{0.52}\text{N}$
10 nm $\text{Al}_{0.32}\text{Ga}_{0.68}\text{N}$
20 nm graded $\text{Al}_x\text{Ga}_{1-x}\text{N:Si}$ $x: 5 \text{ to } 32\% \quad [\text{Si}] = 5 \times 10^{18} \text{ cm}^{-3}$
10 nm GaN:Si $[\text{Si}] = 5 \times 10^{18} \text{ cm}^{-3}$
GaN:Fe Buffer
Sapphire Substrate





RF Model of Measurement Setup

$$a_i = \frac{1}{2} \left(\frac{V_i}{\sqrt{Z_0}} + I_i \sqrt{Z_0} \right)$$

$$b_i = \frac{1}{2} \left(\frac{V_i}{\sqrt{Z_0}} - I_i \sqrt{Z_0} \right)$$

$$S = \begin{bmatrix} S_{11} = \frac{b_1}{a_1} \Big|_{a_2=0} & S_{12} = \frac{b_1}{a_2} \Big|_{a_1=0} \\ S_{21} = \frac{b_2}{a_1} \Big|_{a_2=0} & S_{22} = \frac{b_2}{a_2} \Big|_{a_1=0} \end{bmatrix}$$

$$Z_{out} = Z_{drain} = Z_0 \frac{1 + S_{22}}{1 - S_{22}}$$

$$Z_{in} = Z_{gate} = Z_0 \frac{1 + S_{11}}{1 - S_{11}} \approx \frac{1}{j\omega c_g}$$

$$g_m = \frac{1}{Z_0} \frac{S_{21}}{1 + S_{11}}$$

$$f_T \approx \frac{g_m}{c_g}$$